ABSTRACT

This invention discloses a method for changing a configuring ot an error correction code (ECC) logic circuit for performing an error-check of a changed data-width. The method includes the steps of: A) sequentially interconnecting a set of N1 identical error-check blocks where N1 is a first positive integer. And, the method further includes a step B) of reconfiguring the ECC logic circuit by changing the ECC logic circuit to a set of N2 sequentially interconnected circuits comprising N2 of the identical error-check blocks where N2 is a second positive number. In a preferred embodiment, the step of sequentially interconnecting a set of N1 identical error-check blocks is a step of interconnecting the N1 error-check blocks only between sequentially neighboring blocks for transmitting signals only between the neighboring error-check blocks. And, the step of reconfiguring the ECC logic circuit by changing the ECC logic circuit to a set of N2 sequentially interconnected circuits is a step of interconnecting the N2 error-check blocks only between sequentially neighboring blocks for transmitting signals only between the neighboring error-check blocks.